

### DESCRIPTION

The HY62256A/ HY62256A-I is a high-speed, low power and 32,786 x 8-bits CMOS Static Random Access Memory fabricated using Hyundai's high performance CMOS process technology. The HY62256A/ HY62256A-I has a data retention mode that guarantees data to remain valid at the minimum power supply voltage of 2.0 volt. Using the CMOS technology, supply voltages from 2.0 to 5.5volt has little effect on supply current in the data retention mode. The HY62256A/HY62256A-I is suitable for use in low voltage operation and battery back-up application.

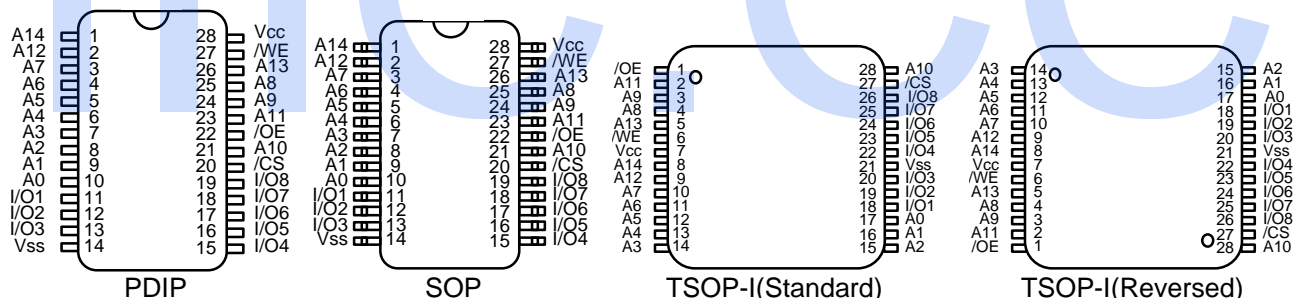
### FEATURES

- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Low power consumption
- Battery backup(L/LL-part)
  - 2.0V(min.) data retention
- Standard pin configuration
  - 28 pin 600 mil PDIP
  - 28 pin 330mil SOP
  - 28 pin 8x13.4 mm TSOP-I (Standard and Reversed)

Product No.	Voltage (V)	Speed (ns)	Operation Current(mA)	Standby Current(uA)			Temperature (jÉ)
				L	LL		
HY62256A	5.0	55/70/85	50	1mA	100	25	0~70(Normal)
HY62256A-I	5.0	55/70/85	50	1mA	100	-	-40~85(E.T.)

Note 1. E.T. : Extended Temperature, Normal : Normal Temperature  
 2. Current value is max.

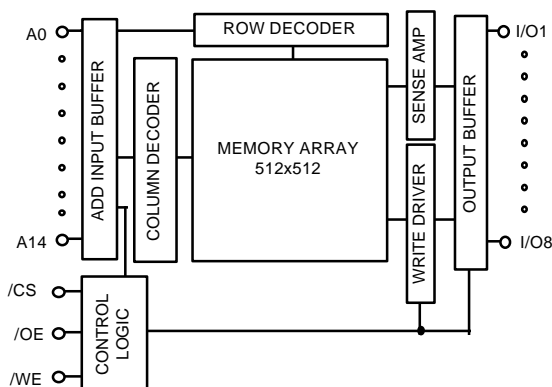
### PIN CONNECTION



### PIN DESCRIPTION

Pin Name	Pin Function
/CS	Chip Select
/WE	Write Enable
/OE	Output Enable
A0 ~ A14	Address Inputs
I/O1 ~ I/O8	Data Input/Output
Vcc	Power(+5.0V)
Vss	Ground

### BLOCK DIAGRAM



**ORDERING INFORMATION**

Part No.	Speed	Power	Temp.	Package
HY62256AP	55/70/85			PDIP
HY62256ALP	55/70/85	L-part		PDIP
HY62256ALLP	55/70/85	LL-part		PDIP
HY62256AJ	55/70/85			SOP
HY62256ALJ	55/70/85	L-part		SOP
HY62256ALLJ	55/70/85	LL-part		SOP
HY62256AT1	55/70/85			TSOP-I Standard
HY62256ALT1	55/70/85	L-part		TSOP-I Standard
HY62256ALLT1	55/70/85	LL-part		TSOP-I Standard
HY62256AR1	55/70/85			TSOP-I Reversed
HY62256ALR1	55/70/85	L-part		TSOP-I Reversed
HY62256ALLR1	55/70/85	LL-part		TSOP-I Reversed
HY62256AP-I	55/70/85		E.T.	PDIP
HY62256ALP-I	55/70/85	L-part	E.T.	PDIP
HY62256AJ-I	55/70/85		E.T.	SOP
HY62256ALJ-I	55/70/85	L-part	E.T.	SOP
HY62256AT1-I	55/70/85		E.T.	TSOP-I
HY62256ALT1-I	55/70/85	L-part	E.T.	TSOP-I
HY62256AR2-I	55/70/85		E.T.	TSOP-I Reversed
HY62256ALR2-I	55/70/85	L-part	E.T.	TSOP-I Reversed

**ABSOLUTE MAXIMUM RATING (1)**

Symbol	Parameter	Rating	Unit	Remark
V <sub>CC</sub> , V <sub>IN</sub> , V <sub>OUT</sub>	Power Supply, Input/Output Voltage	-0.5 to 7.0	V	
T <sub>A</sub>	Operating Temperature	0 to 70	°C	HY62256A
		-40 to 85	°C	HY62256A-I
T <sub>STG</sub>	Storage Temperature	-65 to 150	°C	
P <sub>D</sub>	Power Dissipation	1.0	W	
I <sub>OUT</sub>	Data Output Current	50	mA	
TSOLDER	Lead Soldering Temperature & Time	260•10	°C•sec	

**Note**

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS**

 T<sub>A</sub>=0°C to 70°C / T<sub>A</sub>= -40°C to 85°C(E.T.)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Power Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.2	-	V <sub>CC</sub> +0.5	V
V <sub>IL</sub>	Input Low Voltage	-0.5(1)	-	0.8	V

**Note**

- V<sub>IL</sub> = -3.0V for pulse width less than 30ns

**TRUTH TABLE**

/CS	/WE	/OE	MODE	I/O OPERATION
H	X	X	Standby	High-Z
L	H	H	Output Disabled	High-Z
L	H	L	Read	Data Out
L	L	X	Write	Data In

Note :

 1. H=V<sub>IH</sub>, L=V<sub>IL</sub>, X=Don't Care

**DC CHARACTERISTICS**

 V<sub>CC</sub> = 5V ±10%, T<sub>A</sub> = 0°C to 70°C(Normal)/ -40°C to 85°C(E.T.) unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit		
I <sub>LI</sub>	Input Leakage Current	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-1	-	1	μA		
I <sub>LO</sub>	Output Leakage Current	V <sub>SS</sub> ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , /CS = V <sub>IH</sub> or /OE = V <sub>IH</sub> or /WE = V <sub>IL</sub>	-1	-	1	μA		
I <sub>CC</sub>	Operating Power Supply Current	/CS = V <sub>IL</sub> , V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>I/O</sub> = 0mA	-	30	50	mA		
I <sub>CC1</sub>	Average Operating Current	/CS = V <sub>IL</sub> , Min. Duty Cycle = 100%, I <sub>I/O</sub> = 0mA	-	40	70	mA		
I <sub>SB</sub>	TTL Standby Current (TTL Inputs)	/CS = V <sub>IH</sub> V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	-	0.4	2	mA		
I <sub>SB1</sub>	CMOS Standby Current (CMOS Inputs)	HY62256A	/CS ≤ V <sub>CC</sub> - 0.2V V <sub>IN</sub> ≤ 0.2V or V <sub>IN</sub> ≤ V <sub>CC</sub> - 0.2V		-	-	1	mA
		L		-	2	100	μA	
		LL		-	1	25	μA	
		L		-	2	100	μA	
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1mA	-	-	0.4	V		
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -1mA	2.4	-	-	V		

 Note : Typical values are at V<sub>CC</sub> = 5.0V, T<sub>A</sub> = 25°C

**AC CHARACTERISTICS**

V<sub>CC</sub> = 5V ± 10%, T<sub>A</sub> = 0 °C to 70 °C (Normal) / -40 °C to 85 °C (E.T.) unless otherwise specified.

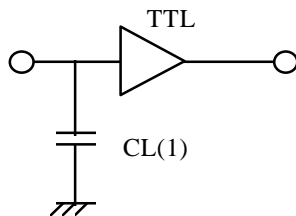
#	Symbol	Parameter	-55		-70		-85		Unit
			Min.	Max.	Min.	Max.	Min	Max.	
<b>READ CYCLE</b>									
1	t <sub>RC</sub>	Read Cycle Time	55	-	70	-	85	-	ns
2	t <sub>AA</sub>	Address Access Time	-	55	-	70	-	85	ns
3	t <sub>ACS</sub>	Chip Select Access Time	-	55	-	70	-	85	ns
4	t <sub>OE</sub>	Output Enable to Output Valid	-	30	-	35	-	45	ns
5	t <sub>CLZ</sub>	Chip Select to Output in Low Z	5	-	5	-	5	-	ns
6	t <sub>OLZ</sub>	Output Enable to Output in Low Z	5	-	5	-	5	-	ns
7	t <sub>CHZ</sub>	Chip Deselection to Output in High Z	0	20	0	30	0	30	ns
8	t <sub>OHZ</sub>	Out Disable to Output in High Z	0	20	0	30	0	30	ns
9	t <sub>OH</sub>	Output Hold from Address Change	5	-	5	-	5	-	ns
<b>WRITE CYCLE</b>									
10	t <sub>WC</sub>	Write Cycle Time	55	-	70	-	85	-	ns
11	t <sub>CW</sub>	Chip Selection to End of Write	50	-	65	-	75	-	ns
12	t <sub>AW</sub>	Address Valid to End of Write	50	-	65	-	75	-	ns
13	t <sub>AS</sub>	Address Set-up Time	0	-	0	-	0	-	ns
14	t <sub>WP</sub>	Write Pulse Width	40	-	50	-	55	-	ns
15	t <sub>WR</sub>	Write Recovery Time	0	-	0	-	0	-	ns
16	t <sub>WHZ</sub>	Write to Output in High Z	0	20	0	30	0	30	ns
17	t <sub>DW</sub>	Data to Write Time Overlap	25	-	35	-	40	-	ns
18	t <sub>DH</sub>	Data Hold from Write Time	0	-	0	-	0	-	ns
19	t <sub>OW</sub>	Output Active from End of Write	5	-	5	-	5	-	ns

**AC TEST CONDITIONS**

T<sub>A</sub> = 0 °C to 70 °C (Normal) / -40 °C to 85 °C (E.T.) unless otherwise specified.

PARAMETER		VALUE
Input Pulse Level		0.8V to 2.4V
Input Rise and Fall Time		5ns
Input and Output Timing Reference Levels		1.5V
Output Load	70/85/100ns	CL = 100pF + 1TTL Load
	55ns	CL = 50pF + 1TTL Load

**AC TEST LOADS**



Note : Including jig and scope capacitance

### CAPACITANCE

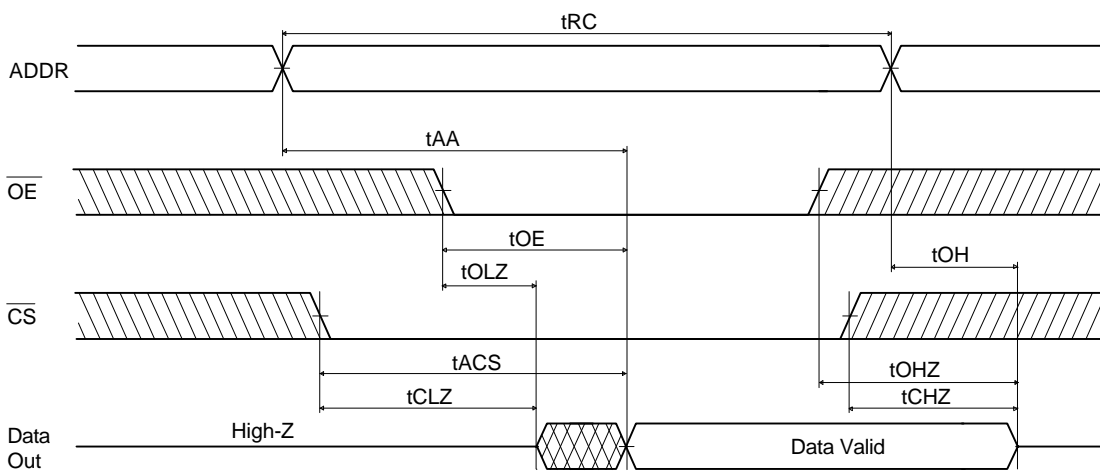
$T_A = 25^\circ\text{C}$ ,  $f = 1.0\text{MHz}$

Symbol	Parameter	Condition	Max.	Unit
$C_{IN}$	Input Capacitance	$V_{IN} = 0V$	6	pF
$C_{I/O}$	Input /Output Capacitance	$V_{I/O} = 0V$	8	pF

Note : These parameters are sampled and not 100% tested

### TIMING DIAGRAM

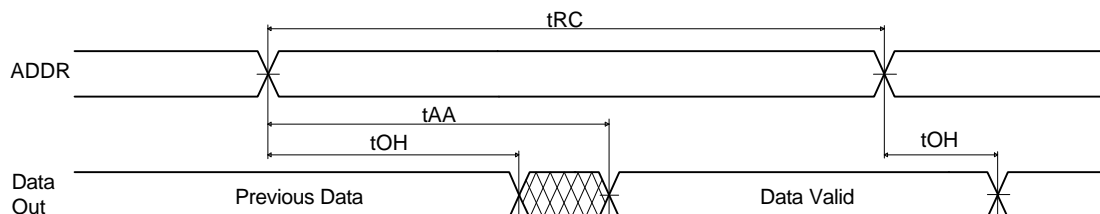
#### READ CYCLE 1



Note(READ CYCLE):

1.  $t_{CHZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition,  $t_{CHZ}$  max. is less than  $t_{CLZ}$  min. both for a given device and from device to device.
3.  $\overline{WE}$  is high for the read cycle.

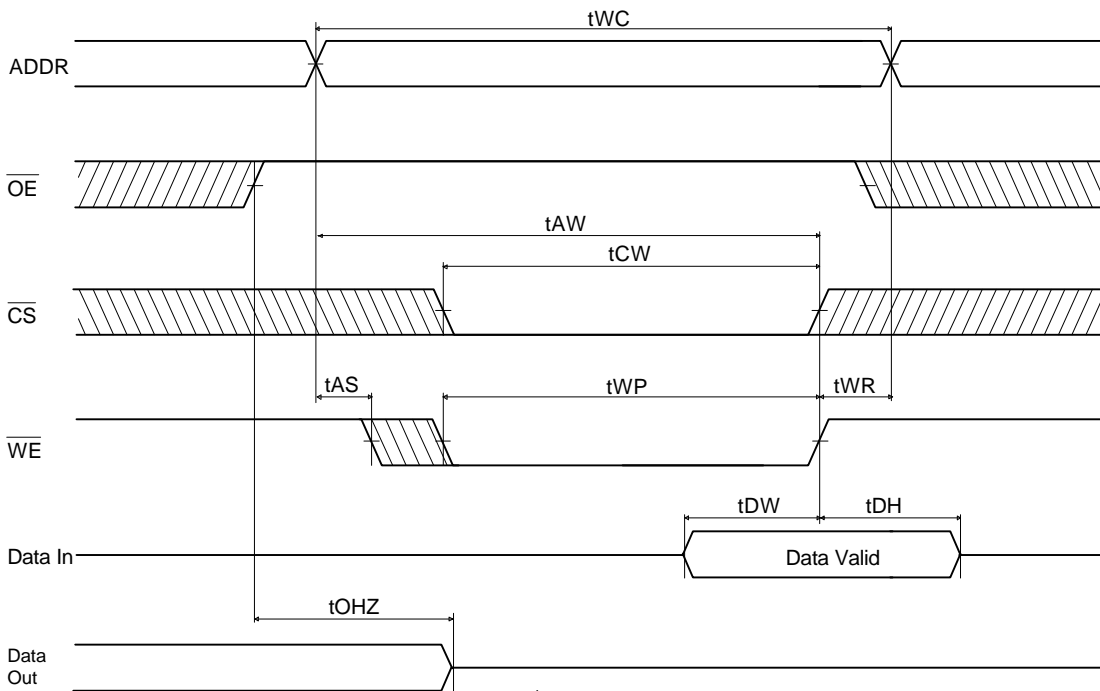
#### READ CYCLE 2



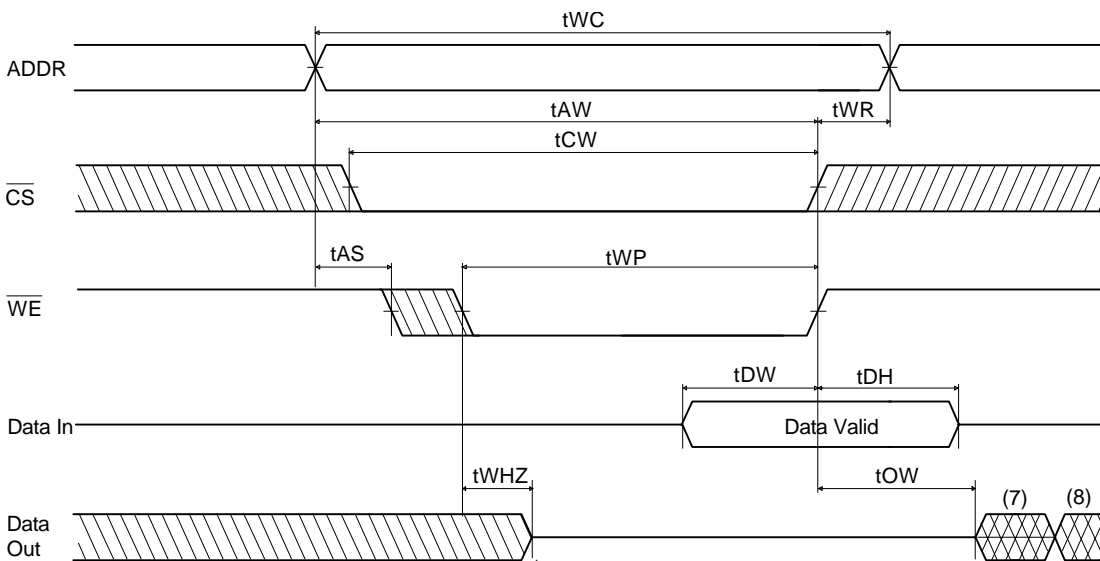
Note(READ CYCLE):

1.  $\overline{WE}$  is high for the read cycle.
2. Device is continuously selected  $\overline{CS} = V_{IL}$ .
3.  $\overline{OE} = V_{IL}$ .

**WRITE CYCLE 1(/OE Clocked)**



**WRITE CYCLE 2 (/OE Low Fixed)**



**Notes(WRITE CYCLE):**

1. A write occurs during the overlap of a low /CS and a low /WE. A write begins at the latest transition among /CS going low and /WE going low: A write ends at the earliest transition among /CS going high and /WE going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the later of /CS going low to the end of write .
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  is applied in case a write ends as /CS, or /WE going high.
5. If /OE and /WE are in the read mode during this period, and the I/O pins are in the output low-Z state, input of opposite phase of the output must not be applied because bus contention can occur.
6. If /CS goes low simultaneously with /WE going low, or after /WE going low, the outputs remain in high impedance state.
7. DOUT is the same phase of latest written data in this write cycle.
8. DOUT is the read data of the new address.

### DATA RETENTION CHARACTERISTIC

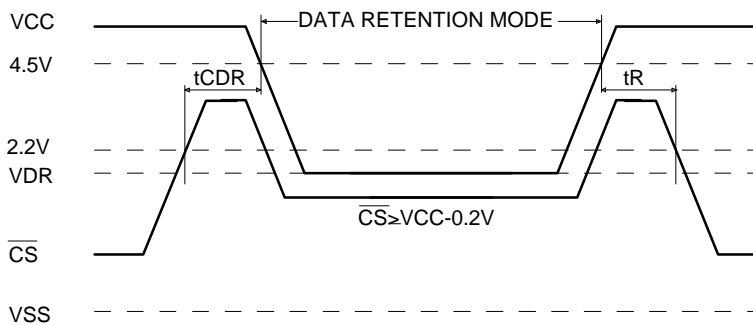
TA=0°C to 70°C (normal)/-40°C to 85°C(E.T.)

Symbol	Parameter		Test Condition		Min	Typ	Max	Unit
VDR	Vcc for Data Retention		/CS; $\hat{A}V_{cc}-0.2V, V_{ss}; \hat{A}V_{IN}; \hat{A}V_{cc}$		2	-	-	V
ICCDR	Data Retention Current	HY62256A	$V_{cc} = 3.0V,$ $/CS; \hat{A}V_{cc} - 0.2V$	L	-	1	50	$\mu A$
				LL	-	1	15(2)	$\mu A$
		HY62256A-I		L	-	1	50	$\mu A$
tCDR	Chip Disable to Data Retention Time		See Data Retention Timing Diagram		0	-	-	ns
tR	Operating Recovery Time				tRC(3)	-	-	ns

#### Notes

1. Typical values are under the condition of TA = 25°C.
2. 3 $\mu A$  max. at TA=0°C to 40°C.
3. tRC is read cycle time.

### Data Retention Timing Diagram

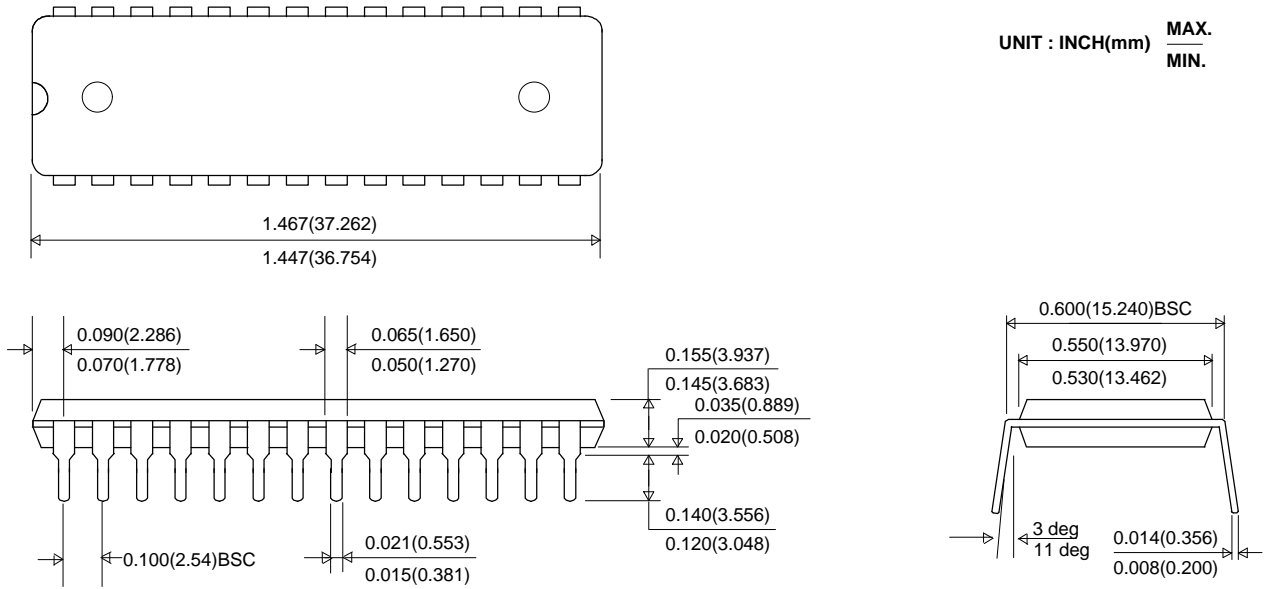


### RELIABILITY SPEC.

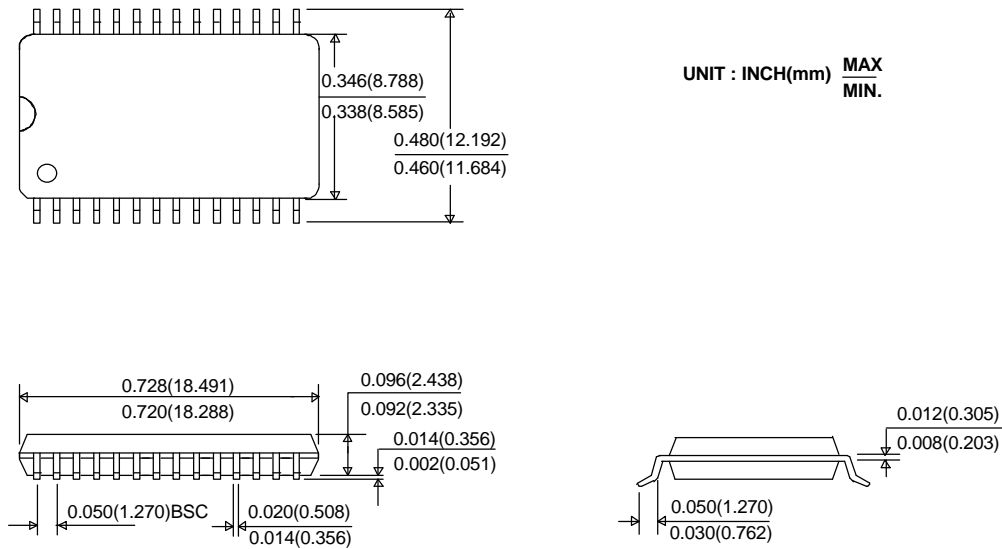
TEST MODE		TEST SPEC.
ESD	HBM	$\hat{A} 2000V$
	MM	$\hat{A} 250V$
LATCH - UP		$\hat{A} -100mA$
		$\hat{A} 100mA$

**PACKAGE INFORMATION**

28pin 600mil Dual In-Line Package(P)

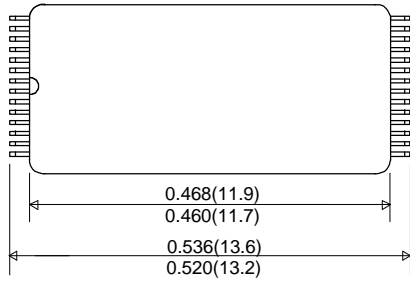


28pin 330mil Small Outline Package(J)

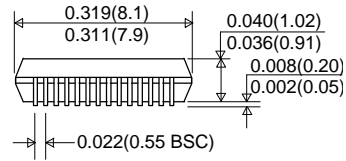
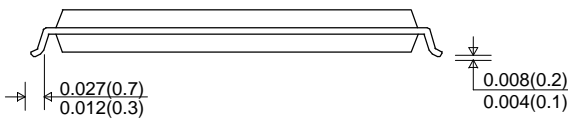




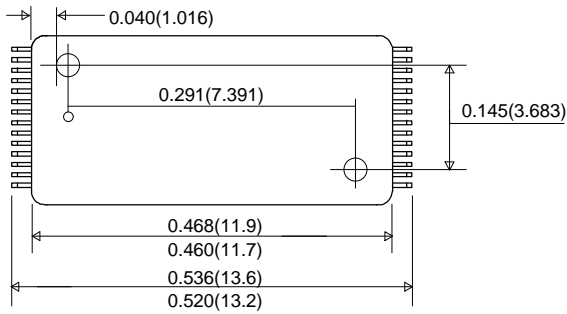
28pin 8x13.4mm Thin Small Outline Package Standard(T1)



UNIT : INCH(mm) **MAX.**  
**MIN.**



28pin 8x13.4mm Thin Small Outline Package Reversed(R1)



UNIT : INCH(mm) **MAX.**  
**MIN.**

